Rasco: Resource Allocation and Scheduling Co-design for DAG Applications on Multicore

Abigail Eisenklam, Robert Gifford, Georgiy A. Bondar*, Yifan Cai, Tushar Sial^T, Linh Thi Xuan Phan, Abhishek Halder^{T*}







The Rise of Data Intensive CPS Tasks

- Tasks in real-time, embedded, and CPS are increasingly data intensive
- Autonomous control, image processing, signal processing, etc.

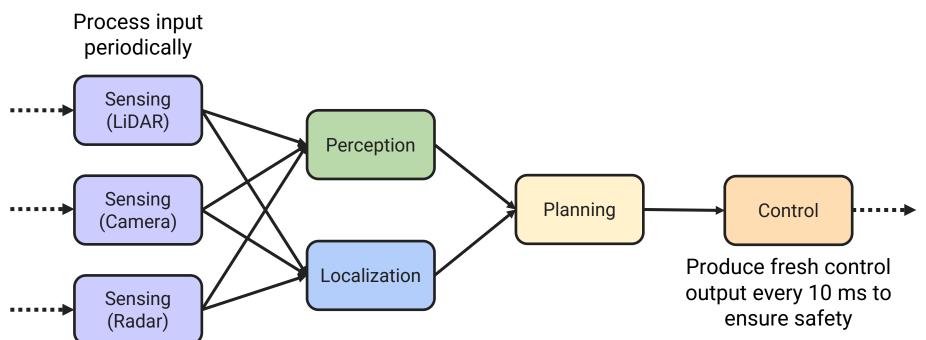


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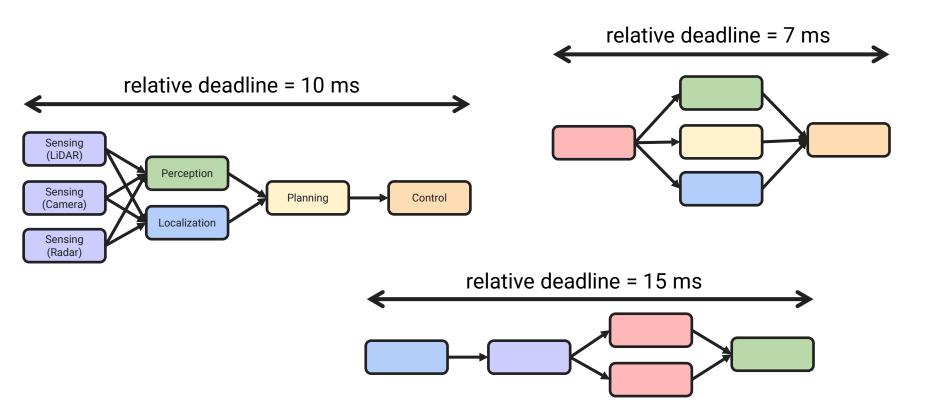
Data Dependencies in CPS

CPS tasks have data dependencies Example: Autoware pipeline Sensing (LiDAR) Perception Sensing Planning Control (Camera) Localization Sensing (Radar)

Data Dependencies in CPS

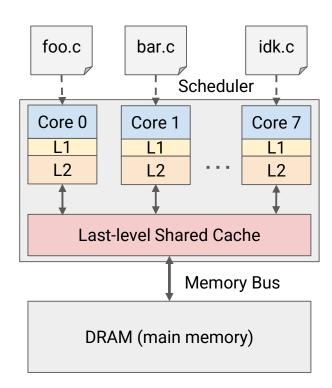


Model: Multiple Periodic DAG Tasks w/ Implicit Deadlines



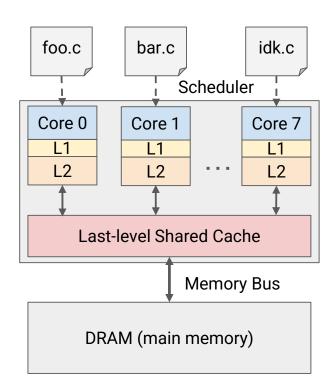
Leveraging Multicore Hardware in CPS

- Multicores exploit inter- and intra-DAG parallelism
 - Lower DAG latency
 - Higher system throughput



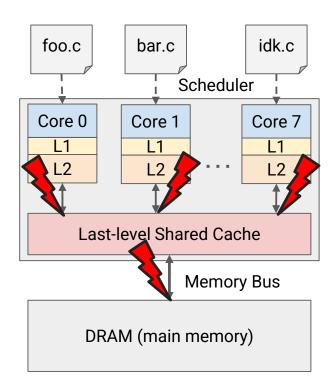
Leveraging Multicore Hardware in CPS

- Multicores exploit inter- and intra-DAG parallelism
 - Lower DAG latency
 - Higher system throughput
- Shared resources such as last-level cache and memory bandwidth are statistically multiplexed
 - Good average case performance



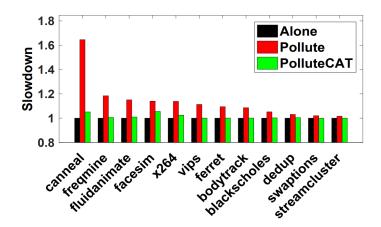
Challenges on Multicore

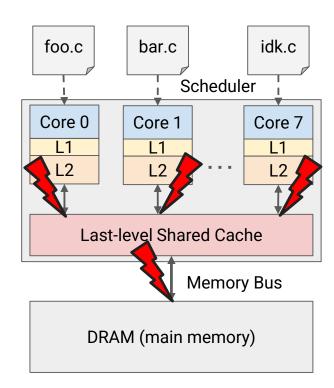
 Contention for shared resources can cause interference between tasks



Challenges on Multicore

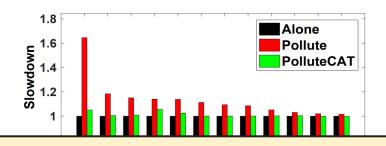
- Contention for shared resources can cause interference between tasks
- Example: WCET slowdown of PARSEC benchmarks due to interference

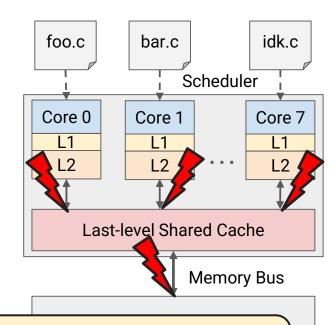




Challenges on Multicore

- Contention for shared resources can cause interference between tasks
- Example: WCET slowdown of PARSEC benchmarks due to interference





Potential interference → overly-conservative worst-case timing analysis → over-provisioning of hardware resources

	Resource aware?	DAG support?	Resource control?	Dynamic control?	Timing analysis?	Takeaway
[Shi et al. RTAS '24] [Casini et al. RTAS '20] [Tessler et al. RTSS '23] [Zhao et al. RTNS '23]	✓	✓	X	X	✓	
CaM [Xu et al. RTAS '19] MMO [Sun et al. ECRTS '25]	✓	X	✓	X	✓	
DNA [Gifford et al. RTAS '20]	√	X	✓	✓	X	

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DNA [Gifford et al. RTAS '20]	✓	X	✓	✓	X	Dynamic allocation breaks timing guarantee

Rasco: Fine-grain Resource Control with Guarantees

	Resource aware?	DAG support?	Resource control?	Dynamic control?	Timing analysis?
Rasco [this work]	✓	✓	√	✓	✓

We want the best of both worlds:

- ✓ Tight worst-case timing analysis via resource isolation
- ✓ Dynamic allocation of resources based on fine-grain needs

Research Questions

- 1. How do we design a task model that enables dynamic resource allocation and worst-case timing analysis?
- 2. Using this model, how do we allocate resources to improve the
 - resource efficiency,
 - average-case latency,
 - and hard real-time schedulability

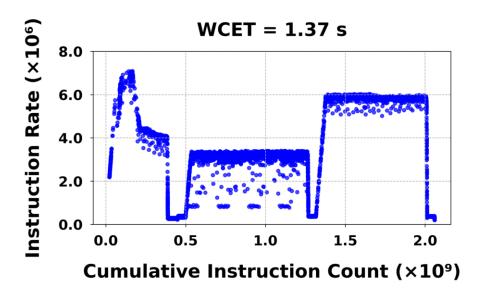
of DAG applications?

Contributions

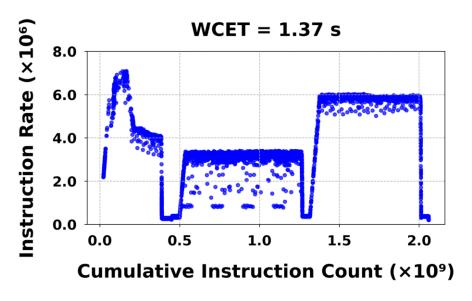
- To answer RQ1, we propose a resource-dependent multi-phase task model which enables worst-case timing analysis under dynamic resource allocation
- To answer RQ2, we develop Rasco, a resource allocation and scheduling codesign algorithm for DAG applications on multicore
- We then implement a prototype of Rasco to evaluate the safety and utility of our approach in a real-time operating system

Talk Outline

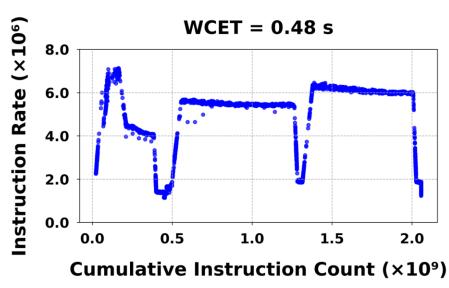
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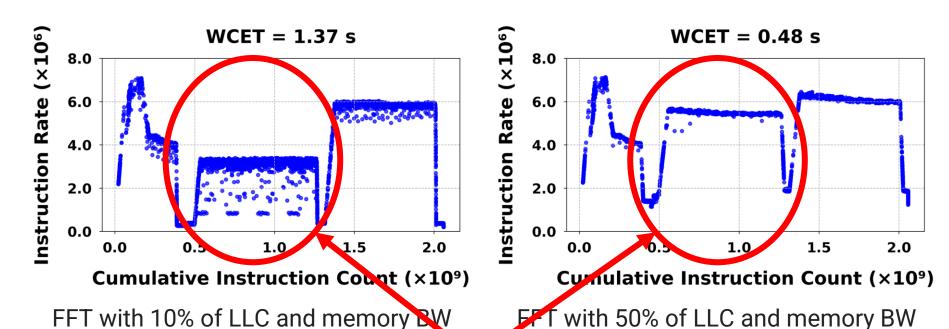
FFT with 10% of LLC and memory BW



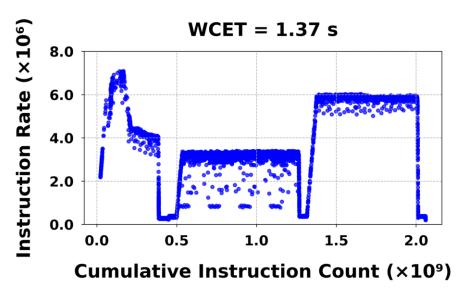
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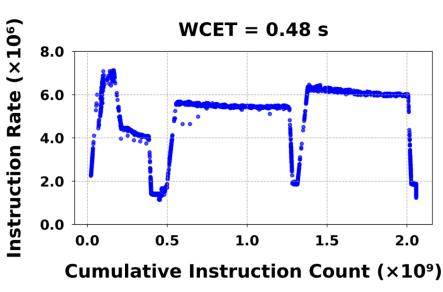
FFT with 50% of LLC and memory BW



Middle phase is highly resource intensive



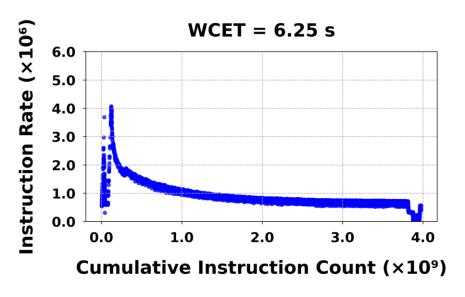
FFT with 10% of LLC and memory BW



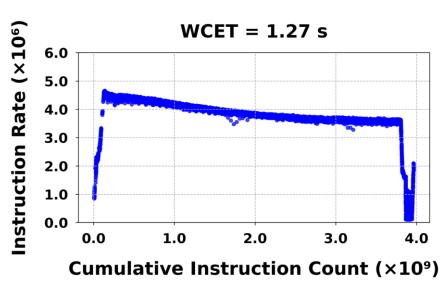
FFT with 50% of LLC and memory BW

- Tasks have different execution phases
- Phases vary in resource intensity

A General Model for Resource-Dependent Phases

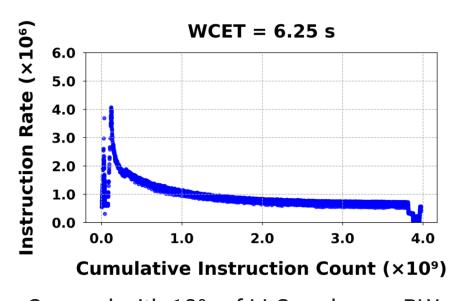


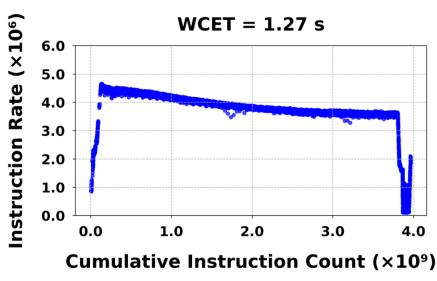
Canneal with 10% of LLC and mem BW



Canneal with 50% of LLC and mem BW

A General Model for Resource-Dependent Phases



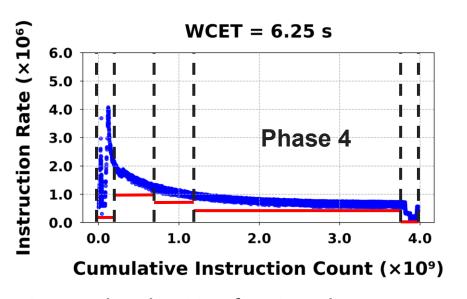


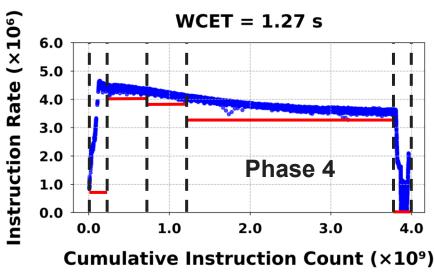
Canneal with 10% of LLC and mem BW

Canneal with 50% of LLC and mem BW

Need a resource-dependent task model that is generalizable, but still tight.

A General Model for Resource-Dependent Phases



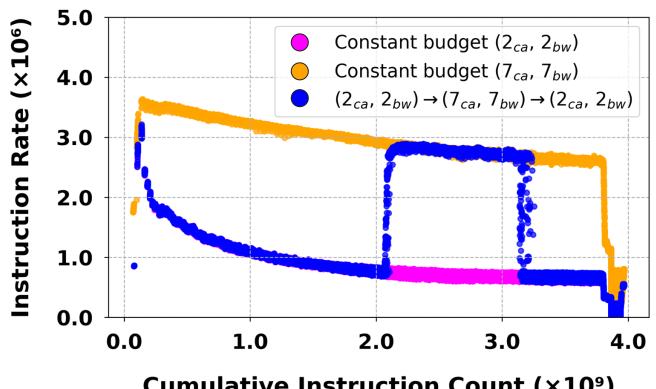


Canneal with 10% of LLC and mem BW

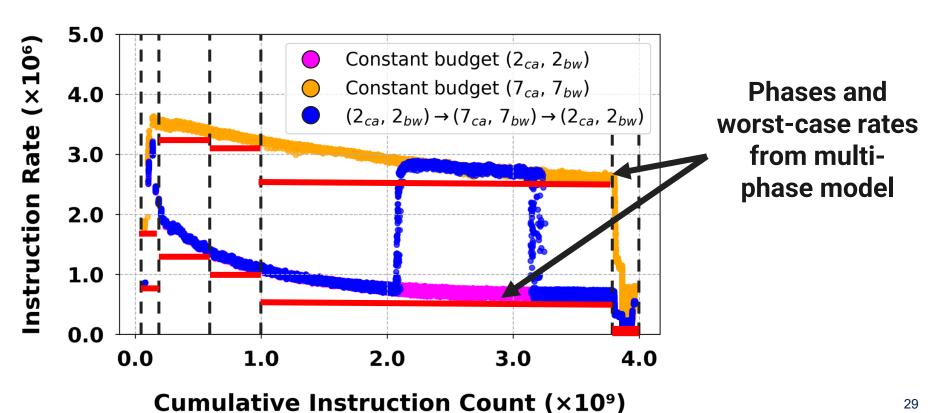
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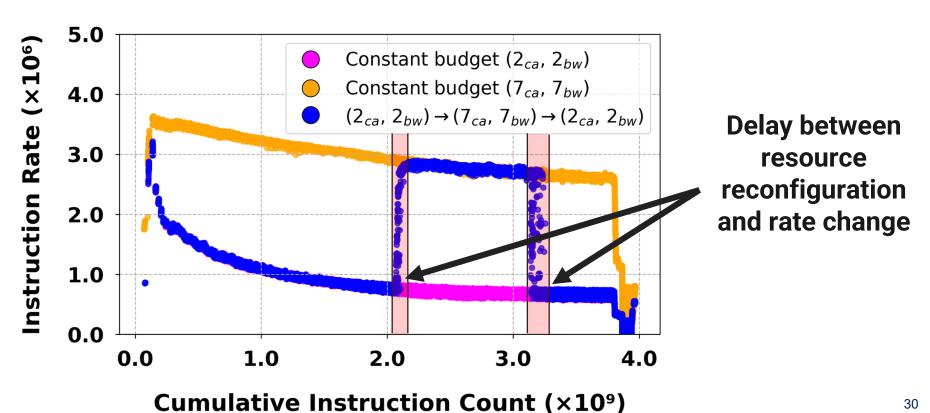
Step 1: use changepoint detection to identify phases

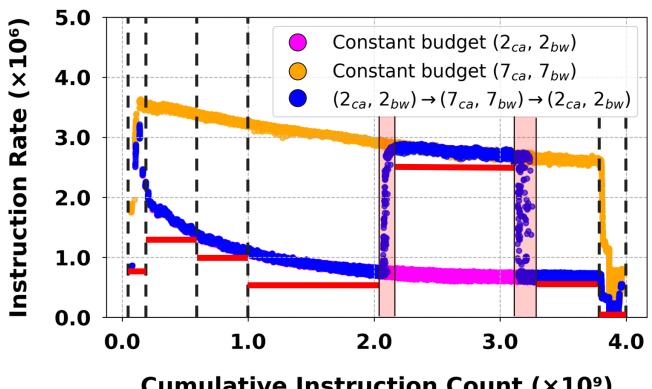
Step 2: compute worst-case instruction rates for each phase



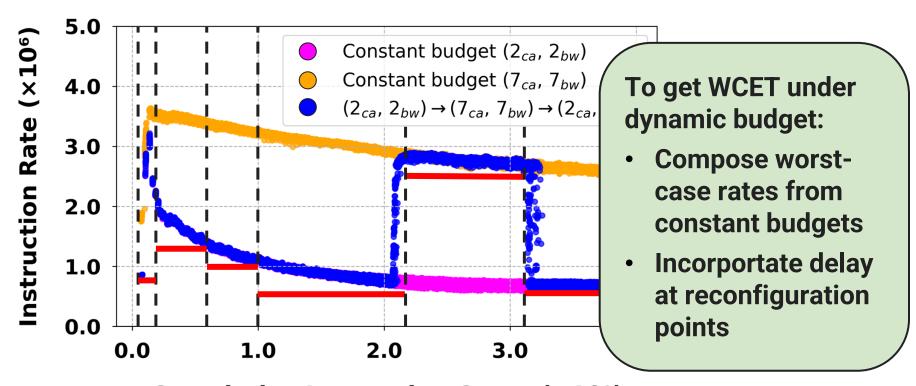
Cumulative Instruction Count (×109)







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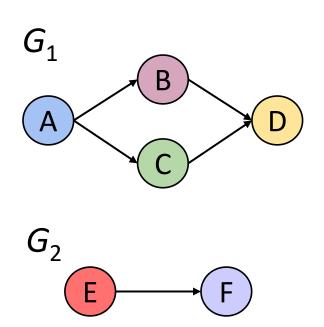


Research Questions

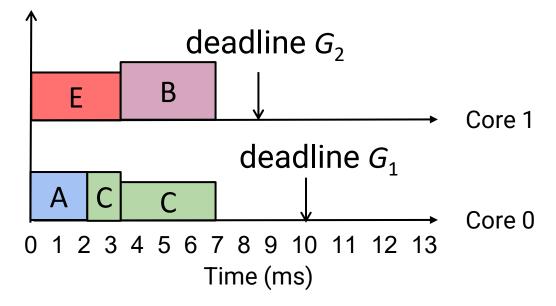
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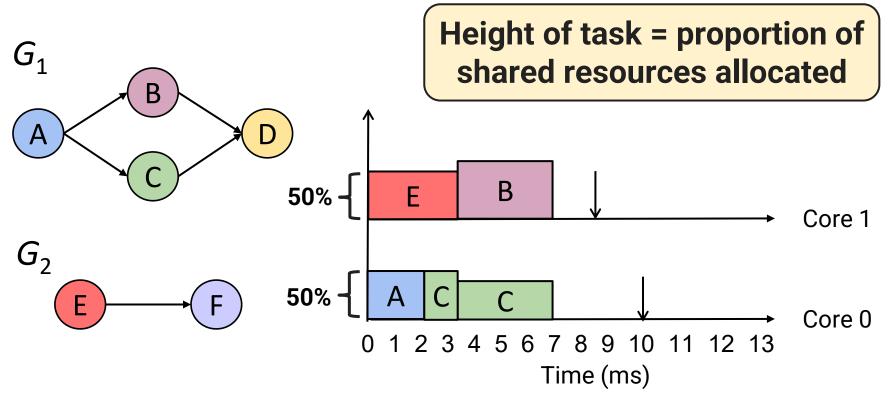
Resource Allocation and Scheduling



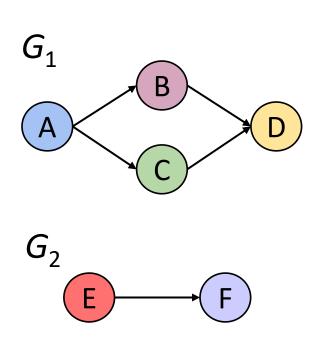
Suppose we are at time t = 7 and need to schedule D and F

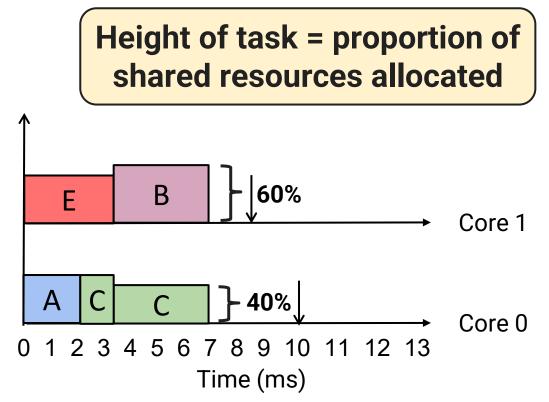


Resource Allocation and Scheduling

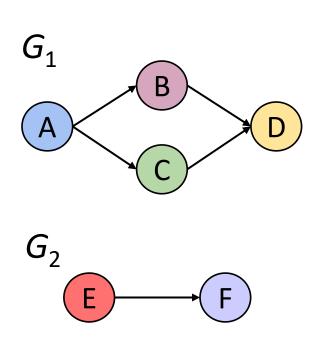


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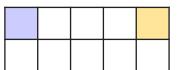


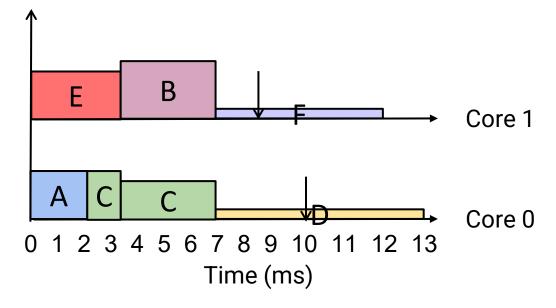


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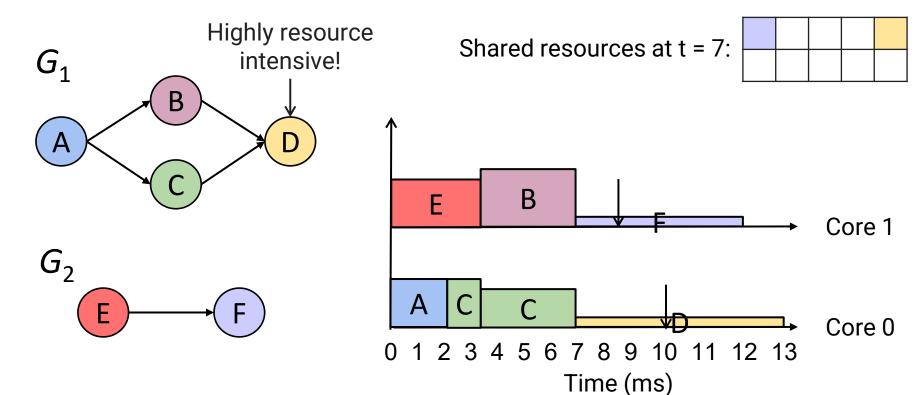


Shared resources at t = 7:

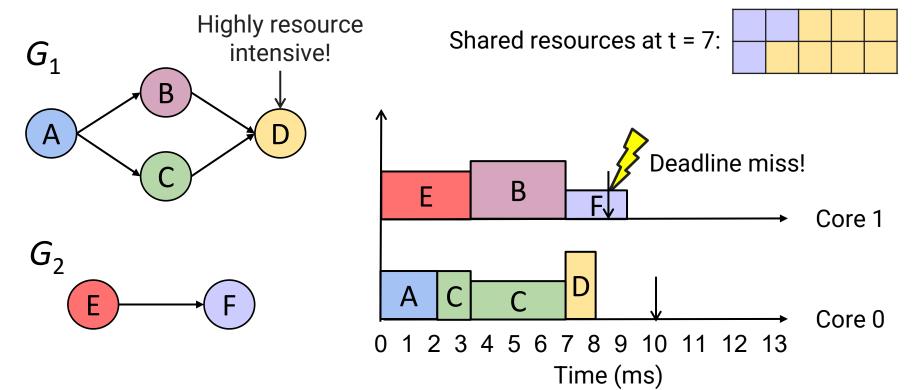




Resource Allocation and Scheduling



Resource Allocation and Scheduling

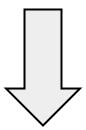


The Case for Co-Design

Maximizing resource efficiency ≠ maximizing schedulability

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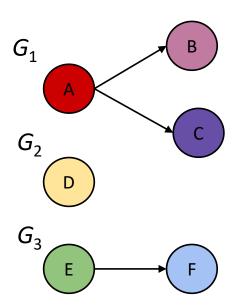


Resource allocation and scheduling must be co-designed.

Talk Outline

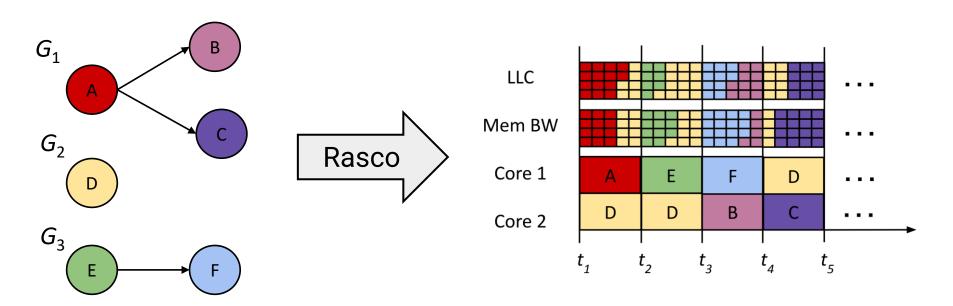
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Rasco Algorithm Overview



Input: periodic DAG tasks and the multi-phase model for each task

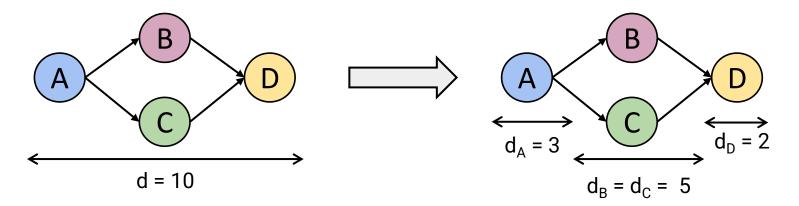
Rasco Algorithm Overview



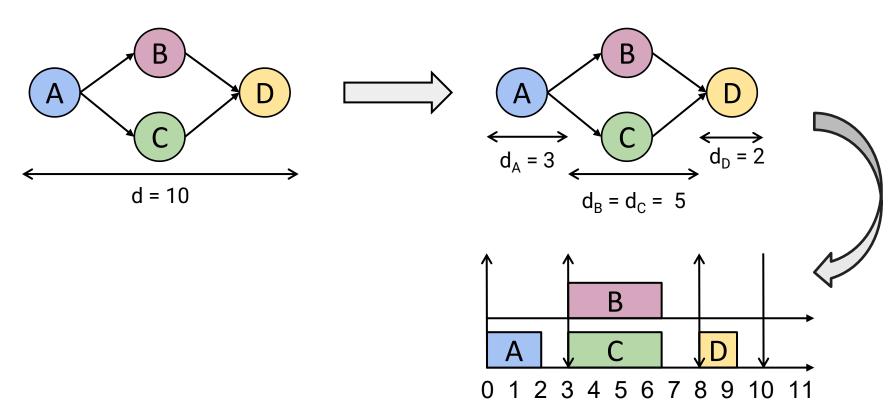
Input: periodic DAG tasks and the multi-phase model for each task

Output: task schedule with partition of shared resources at each scheduling point

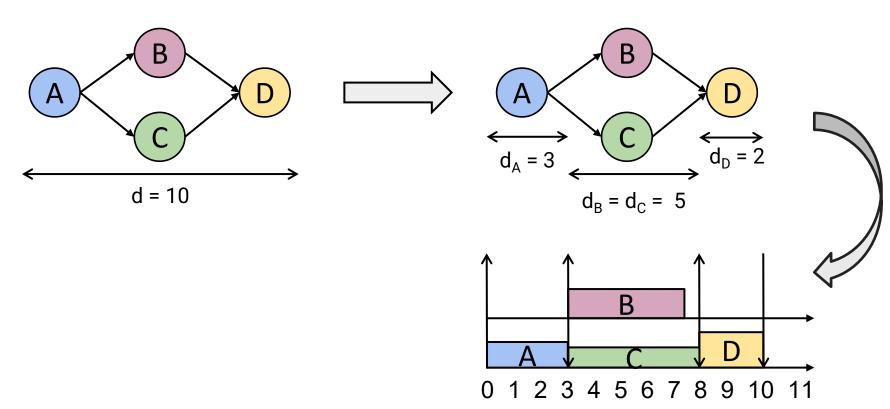
Rasco Pre-Processing: Deadline decomposition



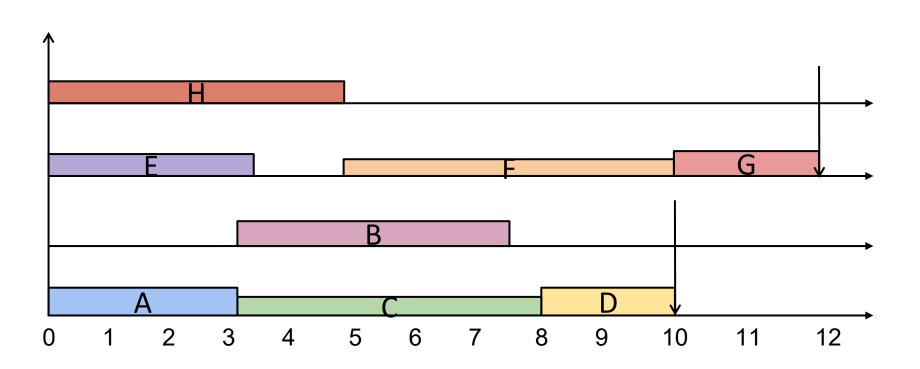
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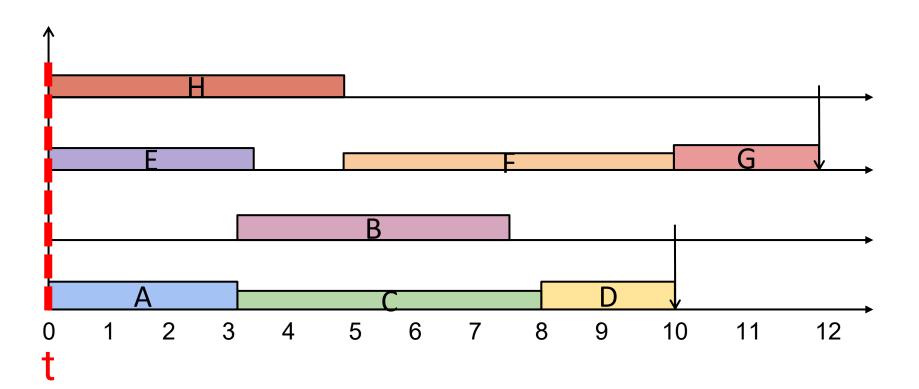
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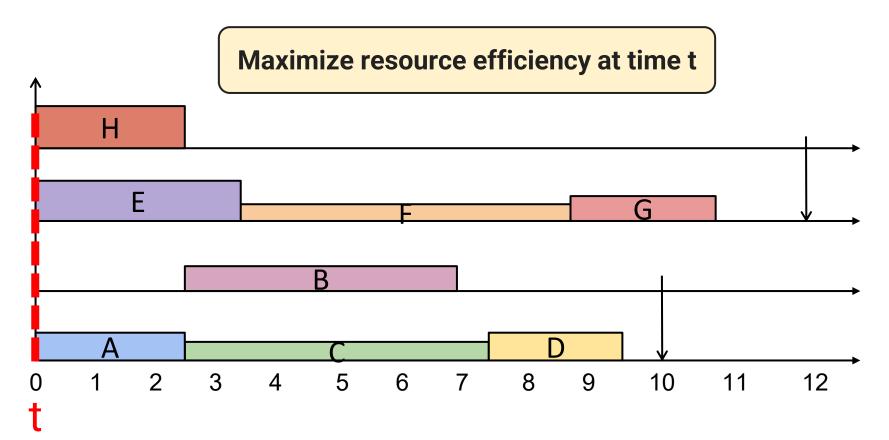
Rasco Pre-Processing: Stack all DAG tasks (G₁, G₂)



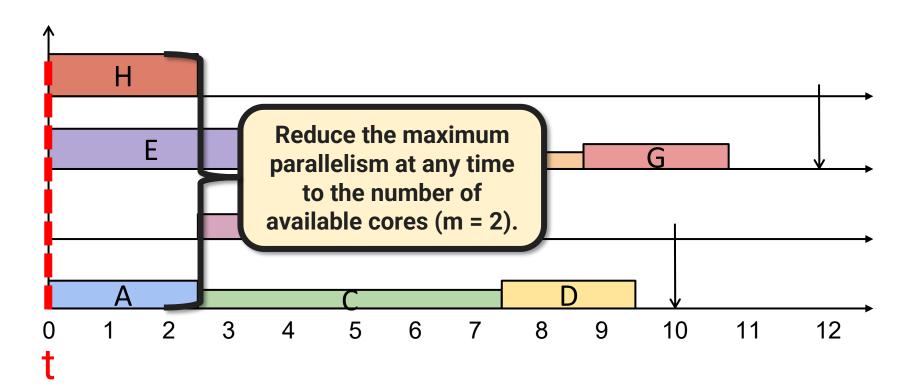
Step 1: Start at t = 0, give out remaining resources at t



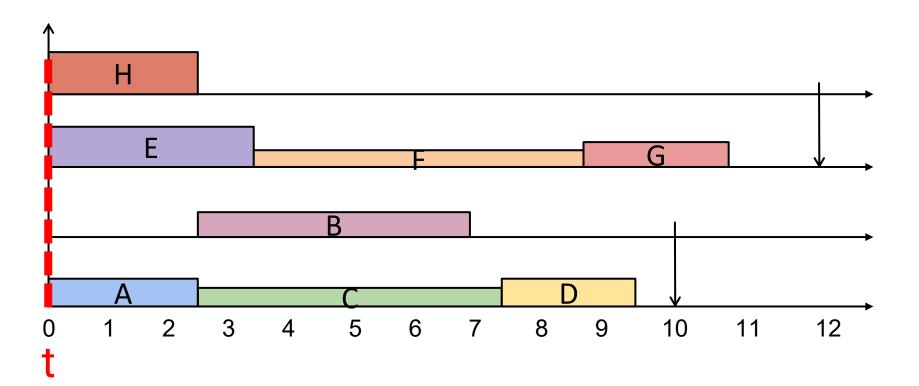
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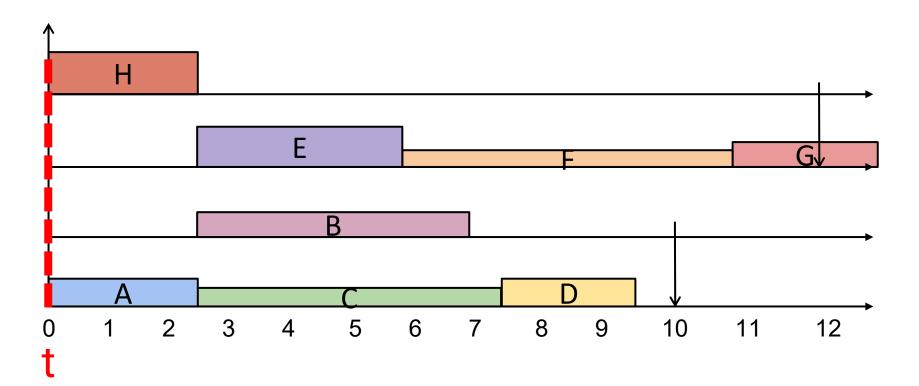
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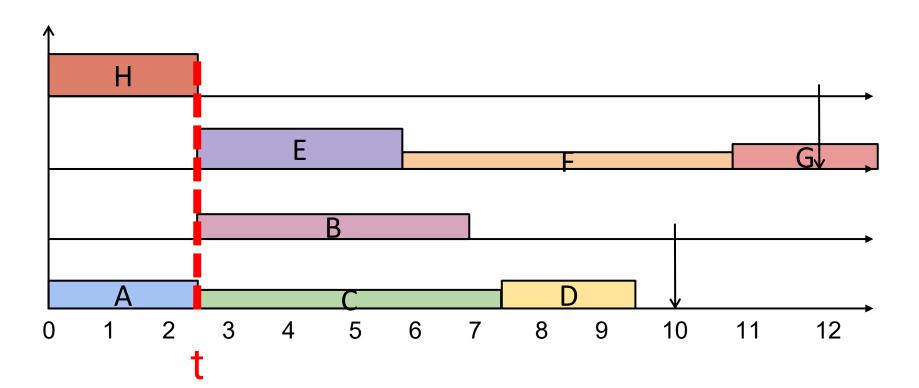


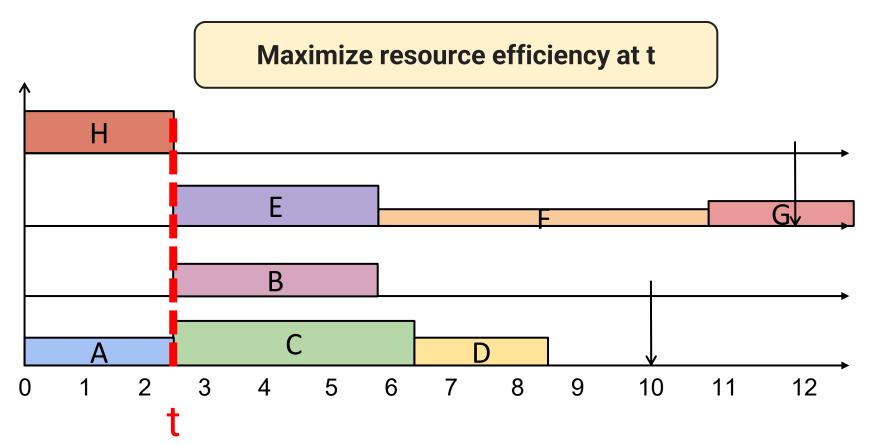
Step 2: Schedule m = 2 tasks with smallest deadlines

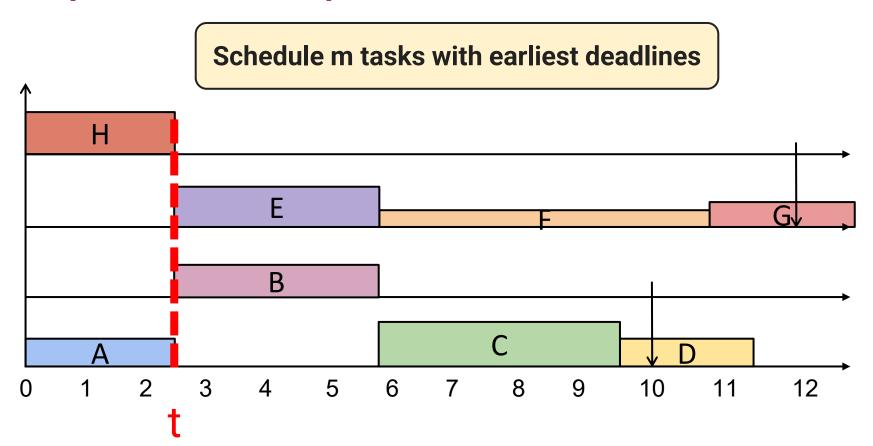


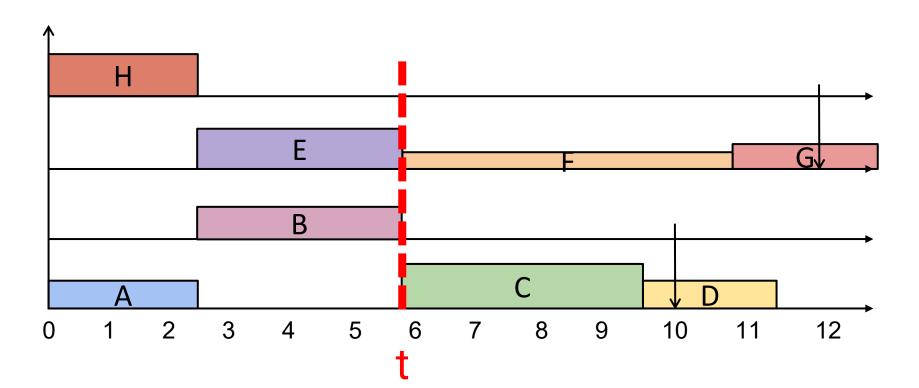
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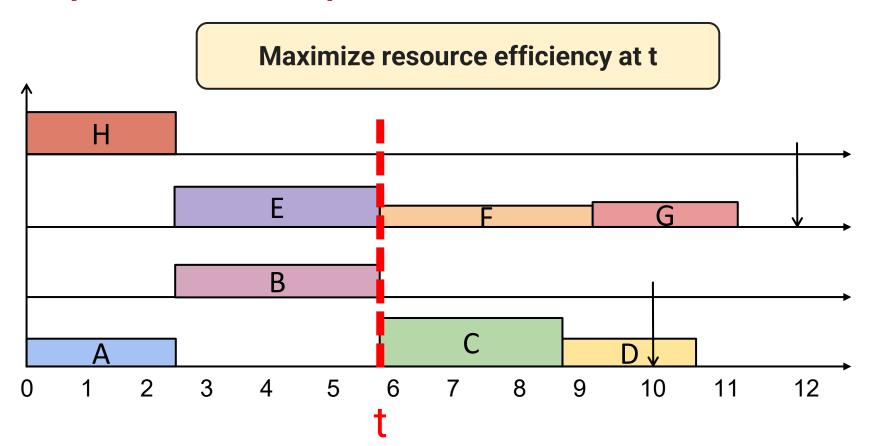


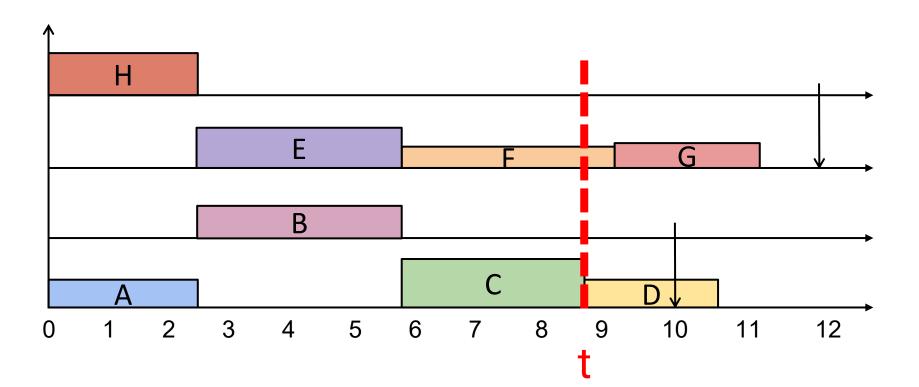


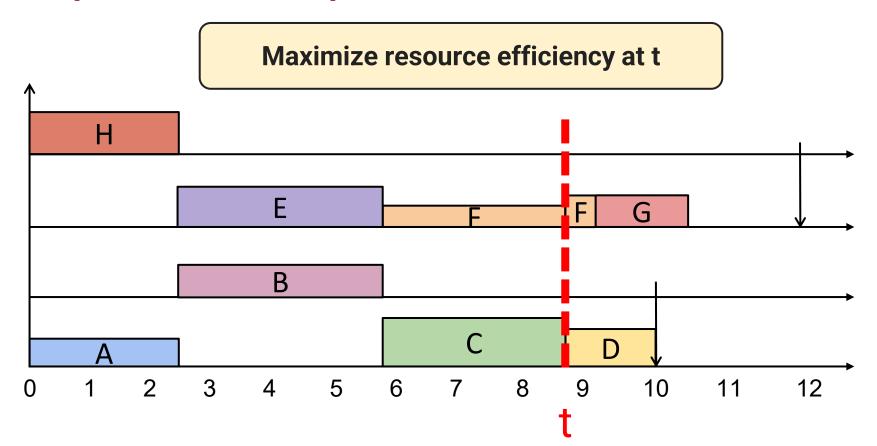




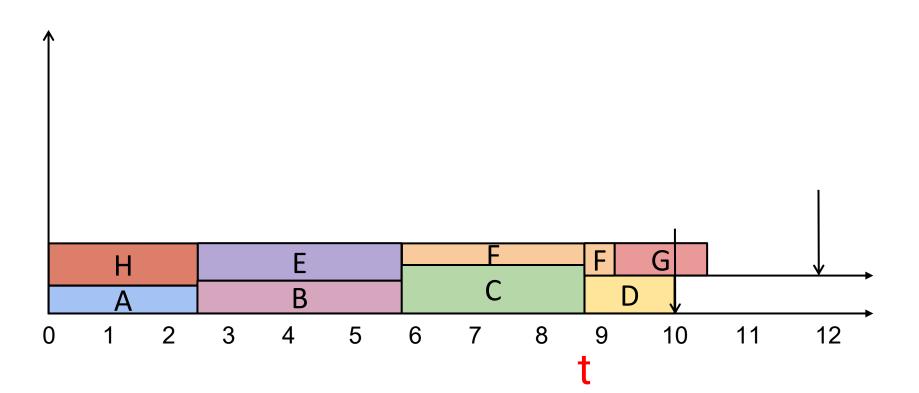




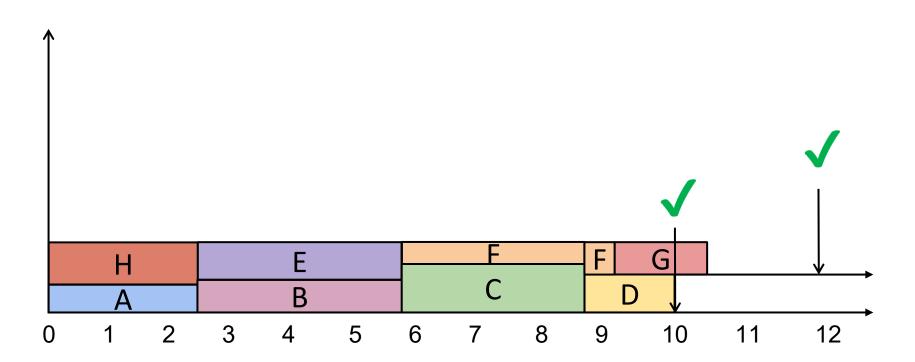




Step 4: Finish and squash onto 2 cores



Step 5: Check if schedulable



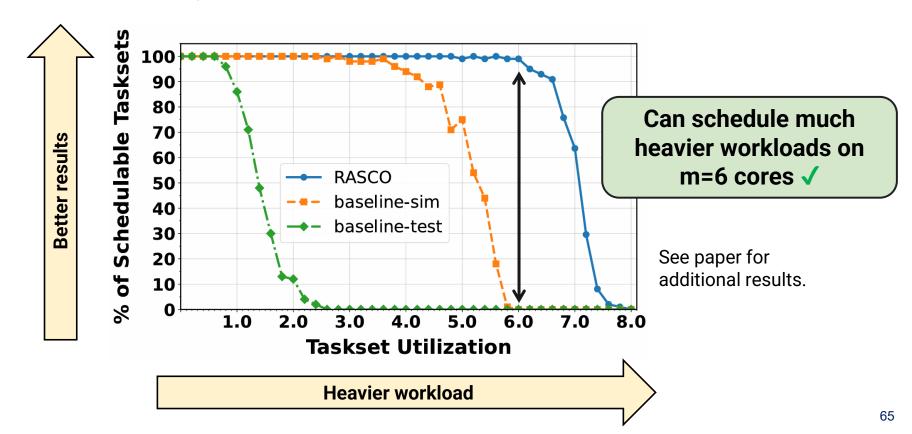
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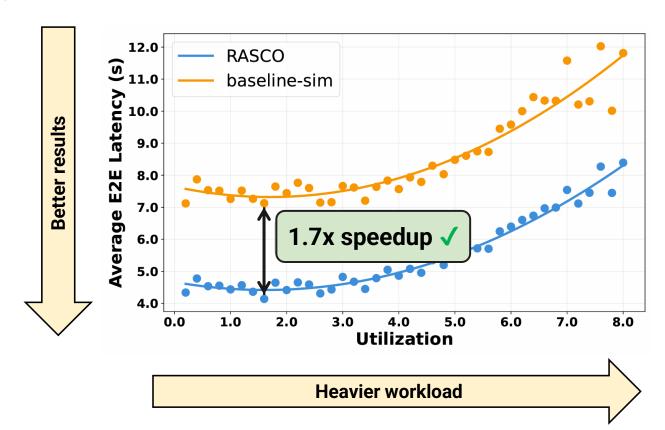
Numerical Evaluation Setup

- Profiled benchmarks from PARSEC and SPLASH2x
- Used Intel's CAT and MemGuard to partition shared resources
- Constructed multi-phase models using changepoint detection
- Randomly generated 100 tasksets per utilization step [X. Dai. dag-gen-rnd]
- Ran Rasco on each taskset
- Compared schedulability and latency against a state-of-the-art deadline decomposition method using even partition of resources to cores
 - Schedulability test: baseline-test
 - Simulated schedule under global EDF: baseline-sim

Schedulability Results



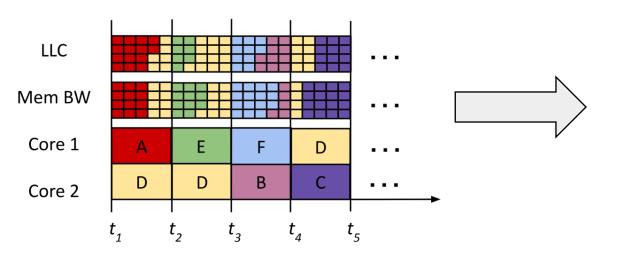
Latency Results



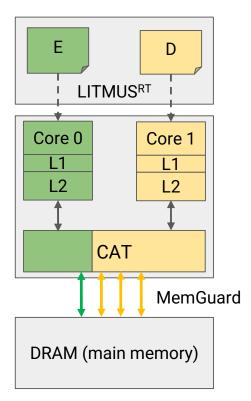
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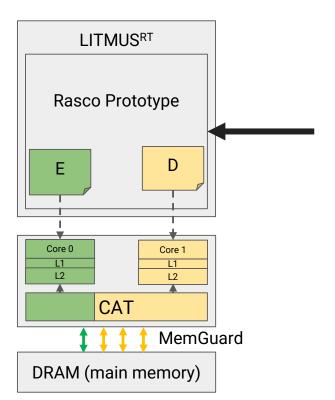
Prototype in LITMUSRT



Prototype state at t₂



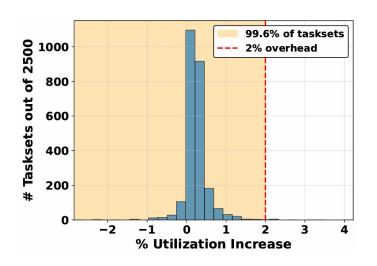
Rasco Prototype Features



- 1. Time-triggered table-driven scheduling in LITMUSRT
- 2. Runtime reconfiguration of CAT + MemGuard in LITMUSRT
- 3. Logic for handling job under-runs
- 4. Early releasing and work stealing

Overhead-Aware Rasco Extension

	Min (µs)	Mean (µs)	99 th (µs)	Max (µs)
Rasco Scheduling	0.02	0.03	0.05	18.10
CAT + MemGuard	1.66	2.53	5.80	23.30

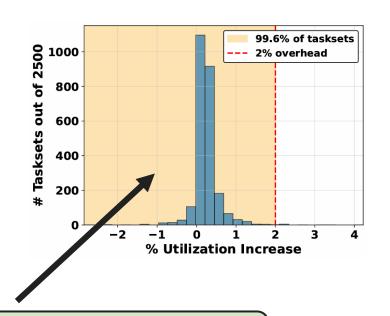




Observed small runtime overheads ✓

Overhead-Aware Rasco Extension

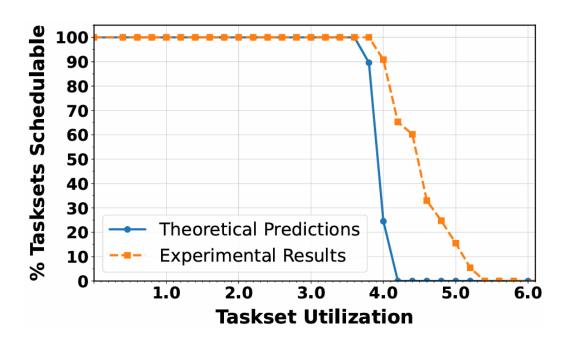
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99.6% of the tasksets had less than 2% overhead ✓

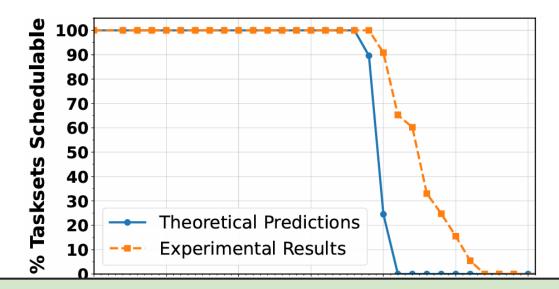
Empirical Evaluation on Prototype

Ran Rasco's output schedules on our prototype



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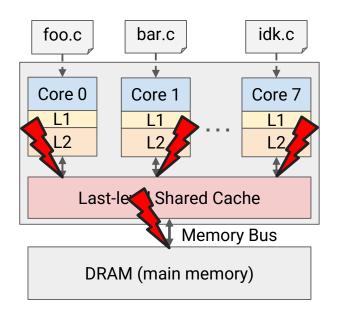


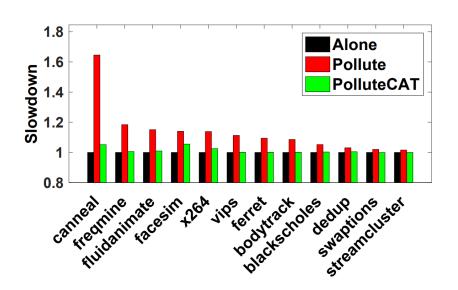
Empirical schedulability always exceeds theoretical guarantee

✓

Recap

- The move to multicore introduces challenges for timing analysis
- Resource contention → overly-conservative analysis → over-provisioning





Recap

 No prior work had achieved the resource efficiency of fine-grained dynamic resource allocation while providing hard real-time guarantees

	Resource aware?	DAG support?	Resource control?	Dynamic control?	Timing analysis?
Rasco	✓	√	✓	✓	✓

Conclusion

- Proposed a resource-dependent multi-phase model which enables worstcase timing analysis under dynamic resource allocation
- Developed a resource allocation and scheduling co-design algorithm for DAG applications on multicore that improves
 - resource efficiency,
 - latency, and
 - schedulability
- Implemented a prototype of Rasco to evaluate the safety and utility of our approach in a real-time operating system

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